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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,330	03/26/2001	Phillip C. Celaya	ONS00149	8912

7590 12/03/2004

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EXAMINER	
PHAN, THIEM D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/817,330	CELAYA ET AL.
	Examiner	Art Unit
	Tim Phan	3729

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19--33,35 & 36* is/are rejected.

7)☒ Claim(s) *34,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/04/04 has been fully considered and made of record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 19-23, 28, 31, 32 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Yano et al (US 6,046,499) hereinafter '499.

As applied to claim 19, the '499 teaches a process of producing a semiconductor package (Cf. Fig. 2, 32), comprising a step of plating (Cf. Col. 7, lines 25 ff.) a conductive material to project outwardly from a second surface (Cf. Fig. 2, 25) of a substrate (Cf. Fig. 2, 13) to form a lead-free first lead (Cf. Fig. 2, 27; col. 7, lines 24 ff.) of the integrated circuit (Cf. Fig. 2, 1).

As applied to claim 20, the '499 teaches a step of mounting a semiconductor die (Cf. Fig. 2, 1) to a first surface (Cf. Fig. 2, 17) of the substrate (Cf. Fig. 2, 13).

As applied to claim 21, the '499 teaches a step of forming a signal path (Cf. Fig. 2, 19 & 31) on the first surface (Cf. Fig. 2, 17) with the conductive material.

As applied to claim 22, the '499 teaches a further step of disposing the conductive material in a via (Cf. Fig. 2, 31; col. 6, lines 63-65) defined by the substrate (Cf. Fig. 2, 13) to extend the signal path from the first surface (Cf. Fig. 2, 17) to the second surface (Cf. Fig. 2, 25) of the substrate.

As applied to claim 23, the '499 teaches a further step of disposing the conductive material on the second surface (Cf. Fig. 2, 25) to extend the signal path from the via (Cf. Fig. 2, 31) to the lead-free first lead (Cf. Fig. 2, 27; col. 7, lines 24 & 25).

As applied to claim 28, the '499 teaches a further step of wire bonding (Cf. Fig. 2, 21) the signal path to a node of the semiconductor die (Cf. Fig. 2, 1) to couple a signal between the node and the lead-free first lead (Cf. Fig. 2, 19; col. 7, lines 6-9).

As applied to claim 31, the '499 teaches a step of plating a bump (Cf. Fig. 2, 27; col. 7, lines 24 ff.) of the conductive material in an outward direction for routing a current through the lead-free first lead (Cf. Fig. 2, 27) that flows parallel to the outward direction of the vias (Cf. Fig. 2, 31).

As applied to claim 32, the '499 teaches a process of producing a semiconductor package (Cf. Fig. 2, 32), comprising the steps of:

- providing a package substrate (Cf. Fig. 2, 13) having a first surface (Cf. Fig. 2, 17) for mounting a semiconductor die (Cf. Fig. 2, 1); and
- plating a bump of conductive material (Cf. Fig. 2, 27; col. 7, lines 24 ff.) to extend outwardly from a second surface (Cf. Fig. 2, 25) of the substrate to form a lead-free lead (Cf. Fig. 2, 27) of the integrated circuit (Cf. Fig. 2, 32).

As applied to claim 36, the '499 teaches a process of producing a semiconductor package (Cf. Fig. 2, 32), comprising the steps of:

- mounting a semiconductor die (Cf. Fig. 2, 1) to a first surface (Cf. Fig. 2, 17) of a substrate (Cf. Fig. 2, 13);
- disposing a conductive material (Cf. Fig. 2, 19) along the first surface (Cf. Fig. 2, 17) and through a via (Cf. Fig. 2, 31; col. 6, lines 63-65) of the substrate to form a signal path of the integrated circuit between the first (Cf. Fig. 2, 17) and a second surface (Cf. Fig. 2, 25) of the substrate; and
- plating the conductive material on the second surface (Cf. Fig. 2, 25) to form a lead-free lead (Cf. Fig. 2, 27; col. 7, lines 24 ff.) of the integrated circuit (Cf. Fig. 2, 1) that is electrically coupled to the signal path (Cf. Fig. 2, 19 & 31).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 24-27, 29, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over the '499.

As applied to claim 24, the '499 teaches a step of forming an access pad (Cf. Col. 4, lines 50 & 51), inherently known to be conductive material, on the second surface (Cf. Fig. 2, 25) or between the bumps (Cf. Fig. 2, 27; col. 4, lines 46 ff.) and the substrate (Cf. Fig. 2, 13), except for plating a conductive material on the access pad.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to plate the conductive material on the access pad, since it was known in the art that the conductive bumps that are connected to the access pad (Cf. col. 4, lines 46 ff.) are obtained by plating (Cf. Col. 7, lines 24 ff.).

As applied to claims 25, 26 and 29, the '499 teaches the claimed invention, including the step of plating a bump (Cf. Fig. 2, 27; col. 7, lines 25-27) of conductive material on the access pads (Cf. col. 4, line 51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to pattern an opening in the photoresist or solder mask with at certain thickness or height to access the pad, since it was known in the art that a bump is plated at the exposed pad (Cf. Fig. 2, 27; col. 4, line 51; col. 7, lines 25-27).

As applied to claims 27 and 33, the '499 teaches the claimed invention, except plating copper.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to plate copper to form the lead-free lead or conductive connection (Cf. Fig. 2, 27), since it was known in the art that the conductive connection can be made by a additional process of plating gold over copper (Cf. col. 7, lines 25 ff.).

As applied to claim 30, the '499 teaches the claimed invention, except for forming the solder mask after plating.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solder mask after plating in order to protect any exposed track on the second surface (Cf. Fig. 2, 25) of the semiconductor package.

As applied to claim 35, the '499 teaches a step of forming the lead to a height that maintains a spacing between the substrate (Cf. Fig. 2, 13) and the motherboard (Cf. Fig. 2, 15).

Allowable Subject Matter

6. Claims 34, 37 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicants' arguments filed 10/04/04 have been fully considered but they are not all persuasive for the following reasons:

Applicants recite *inter alia* "... Yano does not show a step of plating... Yano only teaches the use of individual spherical balls that are placed ... solder balls arranged ... are connected ... which clearly shows that Yano is teaching only the conventional placement of solder balls ...Yano is only describing a process of making individual spherical balls ... clearly teaching ... separate balls ... later attached to the PCB." (Cf. Remarks, page 8, paragraphs 3 & 4, page 9, paragraphs 1 & 2) and "... plating a conductive material to project outwardly from a second surface ..." (Claim 1), the Patent Office's position, as stated in the preceding Action, was and continues to be that since Yano et al (USPN 6,046,499 hereinafter '499) teach the gold plating on a copper core (Cf. Col. 7, lines 24 ff.) to form lead free solder that protrudes or extends outwardly from the second surface, and that the **arrangement** of solder balls (Cf. Col. 4,

lines 35 ff.) are just to **correspond** with the wires and **nowhere** the '499 teaches the placement of solder balls without being plated.

Applicants' citations: " ...Yano does not teach that the first lead and signal path comprise the same material..." (Cf. Remarks, page 9, paragraph 3), the '499 does indeed teach that the first lead (Cf. '499, Fig. 2, 27; col. 7, lines 25 ff.) and signal path (Cf. '499, Fig. 2, 31; col. 7, lines 18 ff.) comprise the same material of copper.

Applicants' remarks of the following: " ...Yano does not teach disposing the conductive material in the via as is called for in claim 22... claim 23 is allowable over Yano because Yano does not teach disposing the conductive material on the second surface to extend the signal path from the via to the lead-free first lead... claim 24 is allowable over Yano because Yano does not teach forming an access pad on the second surface" (Cf. Remarks, page 10, paragraphs 1 & 2) are traversed by the Patent Office. The '499 (Yano) does indeed teach that the filling material (Cf. Fig. 2, 31) in the via is a conductive paste of copper (Cf. Col. 7, lines 18 ff.) and the disposition of the conductive material on the second surface (Cf. Fig. 2, 25) to extend the signal path from the via (Cf. Fig. 2, 31) to the lead-free first lead (Cf. Fig. 2, 27; col. 7, lines 24 & 25) and the formation of an access pad (Cf. Col. 4, lines 50 & 51) on the second surface.

8. With the remainder of the claims rejected under either 35 USC 102 or 35 USC 103, they stand rejected as carefully articulated in the previous and current Office Action and in Responses to Remarks in paragraph 7 above.

It appears that Applicant fail to recognize the scope of the claims when judged in view of the '499. (Cf. MPEP 2111 and *In re Geuns*, 26 USPQ 2nd 1057 (Fed. Cir. 1993)).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. DEXTER TUGBANG
PRIMARY EXAMINER

Tim Phan
Examiner
Art Unit 3729

tp
December 1, 2004